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METHOD FOR TRANSFERRING IMAGE SIGNALS INTO A MEMORY AND A CIRCUIT SUITABLE FOR THIS.

The invention relates to a method for transferring analog image signals of a CCD camera line by line into the memory (RAM) of an electronic unit working with a digital signal processor (DSP) for image processing, the image data being digitized by means of a video processor (VIP). Furthermore, the invention relates to a clock pulse circuit, which can be used to implement the method and with the help of which the system timing of a DSP or of a microprocessor (CPU) can be switched over synchronized to the clock pulse signal for supplying the timing to other parts of the circuit.

Various possibilities have become known for digitizing the video signals of a CCD camera and for transferring them to computer-internal memory units for further processing. In many cases, image data is transferred to the memory of the image processing unit by means of analog scanning ICs, which are tuned by means of appropriate hardware to the synchronous signals of the BAS signal. However, this generally requires a relatively high expenditure for circuits.

Another solution consists of using a VIP. This has the advantage that the VIP, depending on the type, can be programmed using IIC interfaces and therefore can be used in wide standards. Furthermore, it is advantageous that VIPs can be addressed over chip-select signals. However, in the case of such solutions, the problem arises that the VIP generally is supplied with its own timing and therefore is clocked at a frequency, which is different from that of the DSP. In addition, there is usually a phase shift between the clock speed of the VIP and the system timing of the DSP. This is partially attributable also to the formation of PLL loops in the circuitry of the VIP. In order to mutually tune the time regime of the DSP and the VIP into an image processing system, it is therefore necessary to store the digital data, made

available by the VIP, on an interim basis in a buffer memory, to which the DSP has access. For this purpose, first in/first out (FIFO) memories, for example, are used in practice. The FIFOs can be controlled using appropriate software and hardware solutions. However, as a result of the relatively extensive number of control signals required for this and for handling them, very expensive development tools are needed for circuits in the frequency range of 50 MHz or above, so that the resulting expense cannot be justified for pure communication solutions.

The use of FIFOs to couple systems, the frequencies of which are independent of one another, is disclosed, for example, in DE 41 04 644 A1. Furthermore, the DE 40 12 205 A1 discloses a device for the input of image signals into an image memory, which stores the image signals, which originate from a video recorder and are subject to a signal flow that fluctuate with time, initially in a buffer memory, for inscribing in an image memory.

The US patent 5,163,146 discloses a circuit arrangement for switching over the timing for a microprocessor. This circuit arrangement makes it possible to clock the processor with different clock pulse rates. The circuit serves to reduce the timing for the processor optionally, if this is required for exchanging data with slower system components, such as input and output components, by switching over to a lower clock pulse rate. At the same time, the switching over to the lower timing is accomplished by triggering an interrupt. The complete system, equipped with such a circuit, therefore operates with a timing, which is varied between different clock pulse rates for the entire system. The circuit presented in the patent provides no solution for synchronization problems, which arise, when a possible second timing, deviating with respect to the clock pulse rate, is present in the same system.

US patent 5,197,126 describes a circuit, with which the clock pulse frequency of a graphics processor can be switched over to the clock pulse frequency of a host computer. The circuit is such that the switching over between the two clock

pulse frequencies takes place in each case by inserting a dead time into the timing schedule. This is, however, to be regarded as critical, since such a dead time basically represents an interruption to the clock pulse supply, which in many processor-controlled systems can lead to a system crash. The solution presented in the publication is also not transferable to a system working with a video processor because it assumes that both the graphics processor and the host computer – the host computer in a DMA mode – have direct access to the memory. On the other hand, a video processor is not DMA-capable nor can it directly itself address certain memory areas.

The object of the invention is to provide a process that enables analog image signals to be transferred line-by-line into the memory of an image processing unit while at the same time, in comparison to previously known solutions, the costs of the circuit are reduced. It is a further object of the invention to create a circuit arrangement suitable for carrying out the method.

Pursuant to the invention, the objective is accomplished by a method with the distinguishing features of the main patent claim. Advantageous developments of the method are given by the dependent claims. The inventive circuit, which can be used to switch over the clock pulse, is described by the distinguishing features of claim 3. Advantageous developments of the circuit are given in the dependent claims related to claim 3.

The inventive method, for which the analog image signals are transferred line-by-line from a CCD camera to the RAM of the image processing unit by means of a DSP, is characterized in that, during the transfer of the image data supplied by the VIP into the RAM, the DSP is switched to the clock pulse frequency of the VIP clock and the data provided by the VIP is transferred directly over the data bus into the RAM, dispensing with an intermediate storage.

Pursuant to the invention, this is achieved by switching the DSP, so that the image synchronous signal causes an interrupt to be tripped on the DSP and the interrupt routine for the transfer of the data therefore includes at least the following process steps:

a) Switching the system clock of the DSP to the timing of the VIP, on the basis of the interrupt release signal taking effect at a logic unit serving to switch over the clock pulse frequency,
b) Issuing a RAM address to generate a chip-select signal to address a memory address in the address space of the VIP,
c) Generating and issuing a READ signal by means of the DSP,
d) Incrementing the RAM address last issued by means of the DSP, in each case after the transmission of the image data characterizing a pixel of the image into the RAM.

In this connection, it is essential to the invention that the READ signal, issued by the DSP, takes effect at the RAM as a result of an inversion as a WRITE signal. As a consequence of this, the image data present at the VIP, is read over the data bus as a result of the read signal and is directly recorded in the RAM addressed by means of the WRITE signal.

It is within the meaning of the inventive method that, during the blanking interval, the DSP continues to work with the timing of the VIP which, from the clock pulse frequency, is lower but, after a half image transmitted by the CCD camera by the interlaced scanning method, is switched back to its original system timing by resetting the interrupt release signal.

A circuit, suitable for implementing the method introduced, includes, in addition to the DSP and the RAM, at least a video processor (VIP) for digitizing the image data, a write-read control for the RAM, a first clock supplier pulse for the DSP,

a second clock pulse supplier with a clock pulse for the VIP and the DSP, which is lower than that of the first clock pulse supplier, a data bus as well as a logic unit for switching over the timing. The clock pulse signals of the first and second clock pulse suppliers, as well as the image pixel timing of the VIP and an interrupt release signal from the DSP are supplied to the unit for switching over the timing. As a result of the fact that the logic unit, for switching the timing, in each case, at the same level position of the timing signals supplied to it, takes over the current level of the interrupt release signal and, corresponding to this level, switches the clock pulse signal of the first or second clock pulse supplier to the clocking of the DSP, the DSP is coupled over this logic unit alternately with the first or to the second clock pulse supplier. During the transfer of image data to the RAM, the clock pulse signal of the clock pulse supplier, clocking the VIP, is also switched through with the lower clock pulse rate to the DSP. Simultaneously, READ signals, issued by the DSP, take effect at the RAM as WRITE signals as a result of a previous inversion in the write-read control.

Corresponding to a possible embodiment of the inventive circuit, the clock pulse is supplied to the DSP over the output of a clock pulse separating filter to the logic unit for switching over the timing. The first clock pulse signal is supplied to the clock pulse separating filter over a first input and the second clock pulse signal is supplied to the clock pulse separating filter over a second input. The clock pulse separating filter is connected to the output of a flip-flop over a further input. The flip-flop is wired at its D-input with the interrupt release signal issued by the DSP after an interrupt tripped by the image synchronous signal. Its clock pulse input is connected to the output of an AND gate, connecting the clock pulse signals of the first and second clock pulse supplier as well as the image pixel clock pulse of the VIP with one another.

The setting of the flip-flop and the switching over of the timing associated therewith is achieved by means of the transfer, flank-controlled by means

of the clock pulse input, of the interrupt release signal, which is switched to the D-input of the flip-flop and is put out by the DSP after an interrupt tripped by the image synchronizing signal, and only when the level of the output of the gate in front of the flip-flop changes over, for example, from L to H as a result of the AND connection of the three clock pulse signals (VIP pixel clock, VIP system timing and faster DSP system timing).

In an advantageous development of the circuit, a gate circuit is provided in the input region of the clock pulse separating filter. By means of this gate circuit, by means of which, on the one hand, an AND linkage of the clock pulse signal for the VIP with the output signal of the flip-flop is brought about and, on the other, an AND linkage of the higher clock pulse signal, clocking the DSP during actual image processing, with the inverted output signal of the flip-flop is brought about. At the same time, in this embodiment of the inventive circuit, a gate circuit is provided in the output area of the clock pulse separating filter for the OR connection of the output signals of the gate circuit disposed in the input area of the clock pulse separating filter.

The circuit described makes possible a synchronized switching of the DSP to the lower timing of the VIP, as a result of the AND connection of the three timing signals before they are supplied to the timing input of the flip-flop. However, the danger exists that the resulting output timing, which is to be supplied to the DSP, suffers an undesirable phase shift relative to the clock pulse signal of the VIP due to the gate delay times that arise. To compensate for the gate delay times and/or the phase shift that occurs therefor, the gate circuit, which is provided in the input region of the clock pulse separating filter, is constructed pursuant to an advantageous further development of the invention, in such a manner that the clock pulse signals supplied to the clock pulse separating filter, before their AND linkage with the output signal and/or with the inverted output signal of the flip-flop, are themselves subjected to an inversion and the gate circuit, which is provided for the OR linkage of the output

signals of the input region of the clock pulse separating filter, to realize the OR function, are constructed as a NOR gate, to which an inverter is connected in series.

Pursuant to a further advantageous development of the inventive circuit, a RESET-input of the flip-flop is connected with the D input of the flip-flop for the accelerated switching back to the first clock signal originally clocking the DSP or the CPU. It is furthermore necessary to dispose an inverting gate in the connection between D input and clock pulse input, depending on whether the RESET input of the flip-flop is L active or H active. This is necessary especially if the level, bringing about the RESET of the flip-flop, is complementary to the output level of the flip-flop, which brings about the temporary switching over of the DSP to the slower timing.

The invention is explained in greater detail in the following on the basis of an example. The associated drawing:

Figure 1 shows the logic unit for temporarily switching over the system timing of the DSP to the timing of the VIP.

Figure 2 shows a circuit diagram of the inventive circuit, including the circuit of the timing change-over of Figure 1.

In Figure 1, a possible embodiment of a logic unit 100 for timing change-over is shown, with which the system timing (processing timing), which is high during the processing of the image, can be switched temporarily and in a synchronized manner to the lower timing of a VIP 60. As shown in the circuit, timing is supplied to the DSP 50, pursuant to the invention, over the clock pulse separating filter 1. The clock pulse separating filter 1 has three inputs, 11, 12, 13, the quartz-stabilized timing for clocking the DSP 50 being supplied to a first input 11, the timing of the VIP 60 being supplied to a further input 12 and the output signal of a flip-flop 9 being supplied to a last input 13. The D-input 21 of the flip-flop 2 is wired with the interrupt release signal of the DSP 50, which leads to the H level in case of the

interrupt triggered by the image synchronizing signal at the DSP 50. This H level is transferred by the output 24 of the flip-flop 2, as soon as its clock pulse input 22 of which changes over from the L level to the H level as a result of the AND-linked clock pulse signals at the gate 3. As a result of the conversion of the output signal of flip-flop 2 in the clock pulse separating filter 1, the output of the gate 16, wired with the timing of the VIP 4, leads alternately to the L level or the H level depending on the VIP timing. On the other hand, the output of the other gate 15 in the input region 15, 16 of the clock pulse separating filter 1, to which the quartz-stabilized higher timing is supplied, because of the wiring with the inverted output signal of the flip-flop 2, always to the L level as long as the H level is at the output of the flip-flop 2. Over the OR linkage, realized in the output region 17, 18 clock pulse separating filter 1 and provided by connecting a NOR gate 17 in series with an inverter 18, the clock pulse signal of the VIP 60 is switched through to the output 14 of the logic unit 100 clocking the DSP 50 by connecting an NOR gate in series with OR linkage realized with an inverter. This means that the DSP 50 is clocked with the lower timing of the VIP 60 as long as the interrupt release signal is at the D input 21 of the flip-flop 2.

Since, pursuant to the inventive method, the interrupt release signal is placed in readiness and a READ signal is put out by the DSP 50 issues and supplied to the RAM 70 in inverted form, the digitized image data queued at the data outputs of the VIP 60 are read in over data bus 90 directly by the RAM 70 addressed by the WRITE signal. The data accordingly is transferred to the RAM 70 in accordance with the clock pulse regime of the VIP 60. By means of the end linkage of the timing for the VIP 60 with pixel timing of the latter, as well as with the higher timing in the gate 3, serving for the timing of the DSP 50 for the image processing, a switching over of the rapid DSP timing to the slower VIP timing is achieved and is synchronized with respect to the phase position.

As is furthermore shown by logic unit 100, measures, by means of which gate delay times occurring in circuit 100 are compensated for, are taken by the

VIP timing and the DSP timing in order to assure the synchronicity existing at the instant of changeover. This is accomplished, on the one hand, owing to the fact that the timing of the VIP 60 and the higher processing timing at the corresponding inputs 11, 12 of the clock pulse separating filter 1 are inverted with respect to their phase position. In addition, the OR linkage of the signals formed in its input region 15, 16, required in the output region 17, 18, is brought about by means of an NOR-gate 17 and an inverter 18 connected in series with the gate 17. In this manner, it is achieved the timing, switched through to the output 14 of logic unit 100, is always in phase with the timing of the VIP 60.

An overview of the entire circuit, with which the inventive method, including the logic unit 100 for changing over the timing, can be realized, is shown once again in Figure 2. Three timing signals are supplied to the logic unit 100 for changing over the timing. These are, on the one hand, the high timing for the image processing of, for example, 50 MHz, furthermore the timing clocking the VIP 60 of, for example, 24.576 MHz, as well as the pixel timing of the VIP 60 (SYN-VIP). In addition, as can be seen, an interrupt release lead is brought from the DSP 50 to the circuit 100 for changing over the timing (ISP). The DSP 50, in turn, is supplied over this logic unit 100 with the timing required in each case. When image data is processed or as long as image data does not have to be read in, that is, for example, also within the image gating gap between two half images, said required timing is the higher 50 MHz timing and, and during the transfer of image data from the VIP 60 to the RAM 17, the lower VIP timing. Admittedly, it is conceivable to switch the DSP 50 back to the higher timing even during the line gating signal, but this is less reasonable due to the higher circuitry expense associated therewith.

As can be seen, the DSP 50 is connected to the RAM 70 over a write-read control 80. The latter assures, for instance, that the correct physical RAM address is addressed in each case and, in addition, the conversion of the READ signal into the WRITE signal is brought about during the transfer of data from the VIP 60. With

respect to the physical address in the RAM 70, which is to be addressed in each case for writing or reading, the write-read control 80 sees to it that this address in each case corresponds to the logical address assigned by the DSP 50 or the VIP 60. This is necessary if the two processors 50, 60 work in logically different address spaces.

List of the reference symbols used

10 Timing pulse separating filter

- 11 Timing pulse separating filter input for first timing signal
- 12 Timing pulse separating filter input for second timing signal (VIP timing)
- 13 Timing pulse separating filter input
- 14 Timing pulse separating filter output
- 15 Gate in input area of the timing pulse separating filter
- 16 Gate in input area of the timing pulse separating filter
- 17 Gate in output area of the timing pulse separating filter – NOR gate
- 18 Gate in output area of the timing pulse separating filter – inverter

20 Flip-flop

- 21 D-input flip-flop
- 22 Timing input flip-flop
- 23 RESET-input flip-flop
- 24 Output flip-flop

30 Gate

- 31 Input gate for first timing signal
- 32 Input of gate for second timing signal (VIP timing)
- 33 Input gate for pixel timing from VIP
- 34 Output gate

40 Inverter

50 DSP

60 VIP

70 RAM

80 Write-read control

90 Data bus

100 Logic unit (circuit arrangement) for switching over the timing